WHAT IS CLAIMED IS:

1. A semiconductor apparatus having a logic level decision circuit, the logic level decision circuit comprising:

a first comparison circuit which compares an input signal with a first reference signal corresponding to logic "1" level, and which outputs a first differential signal;

a second comparison circuit which compares the input signal with a second reference signal corresponding to logic "0" level, and which outputs a second differential signal; and

a third comparison circuit which compares output of the first comparison circuit and output of the second comparison circuit, and which decides a logic level of the input signal.

2. A semiconductor apparatus according to claim 1, wherein the logic level decision circuit is an input receiver which decides a logic level of an input signal from an exterior.

3. A semiconductor apparatus according to claim 1, wherein the logic level decision circuit is a sense amplifier circuit which decides a logic level of a reading signal from a memory cell.

4. A semiconductor apparatus according to claim 3, further comprising:

a first memory cell which generates the first

reference signal; and

a second memory cell which generates the second reference signal.

5. A semiconductor apparatus according to claim 4, wherein a signal level of the first reference signal is greater than a signal level of the second reference signal, and the signal level of the first reference signal is a value greater than a maximum value of a distribution of a signal level of the logic "1" level of the input signal, and the signal level of the second reference signal is a value less than a minimum value of a distribution of a signal level of the logic "0" level of the input signal.

6. A semiconductor apparatus according to claim 4, wherein a signal level of the second reference signal is greater than a signal level of the first reference signal, and the signal level of the first reference signal is a value less than a minimum value of a distribution of a signal level of the logic "1" level of the input signal, and the signal level of the second reference signal is a value greater than a maximum value of a distribution of an input level of the logic "0" level.

7. A semiconductor apparatus according to claim 1, wherein

the logic level decision circuit is a voltage input type logic level decision circuit, and

the first comparison circuit is a current mirror type first voltage comparison circuit, and the second comparison circuit is a current mirror type second voltage comparison circuit.

8. A semiconductor apparatus according to claim 1, wherein

the logic level decision circuit is a current input type logic level decision circuit, and

the first comparison circuit is a current mirror type first current comparison circuit, and the second comparison circuit is a current mirror type second current comparison circuit.

9. A semiconductor apparatus according to claim 7, wherein

the first and second voltage comparison circuits each have a pair of transistors for load and a pair of transistors for input,

the respective driving abilities of the pair of transistors for load of the respective first and second voltage comparison circuits are set so as to be the same, and

the driving abilities of the pair of transistors for input of the first voltage comparison circuit and the pair of transistors for input of the second voltage comparison circuit corresponding thereto are set so as to differ in accordance with a relationship of magnitudes of the signal level of the first reference

signal and the signal level of the second reference signal.

10. A semiconductor apparatus according to claim 8, wherein

the first and second current comparison circuits each have a pair of transistors for load and a pair of transistors for input,

the respective driving abilities of the pair of transistors for load of the respective first and second current comparison circuits are set so as to be the same, and

the driving abilities of the pair of transistors for input of the first current comparison circuit and the pair of transistors for input of the second current comparison circuit corresponding thereto are set so as to differ in accordance with a relationship of magnitudes of the signal level of the first reference signal and the signal level of the second reference signal.

11. A semiconductor apparatus according to claim 9, wherein

the signal level of the first reference signal is greater than the signal level of the second reference signal,

among the pair of transistors for input of the first voltage comparison circuit, the driving ability of the transistor at which the first reference signal

is input to a gate thereof is M1, and the driving ability of the transistor at which the input signal is input to a gate thereof is M2, and

among the pair of transistors for input of the second voltage comparison circuit, the driving ability of the transistor at which the input signal is input to a gate thereof is M3, and the driving ability of the transistor at which the second reference signal is input to a gate thereof is M4,

a relationship M1 > M2 = M3 > M4 is established among the driving forces M1 to M4.

12. A semiconductor apparatus according to claim 9, wherein

the signal level of the second reference signal is greater than the signal level of the first reference signal,

among the pair of transistors for input of the first voltage comparison circuit, the driving ability of the transistor at which the first reference signal is input to a gate thereof is M1, and the driving ability of the transistor at which the input signal is input to a gate thereof is M2, and

among the pair of transistors for input of the second voltage comparison circuit, the driving ability of the transistor at which the input signal is input to a gate thereof is M3, and the driving ability of the transistor at which the second reference signal is

input to a gate thereof is M4,

a relationship M4 > M2 = M3 > M1 is established among the driving forces M1 to M4.

13. A semiconductor apparatus according to claim 10, wherein

the signal level of the first reference signal is greater than the signal level of the second reference signal,

among the pair of transistors for input of the first current comparison circuit, the driving ability of the transistor at which current corresponding to the current of the input signal flows is M2, and the driving ability of the transistor at which current corresponding to the current of the first reference signal flows is M3, and

among the pair of transistors for input of the second current comparison circuit, the driving ability of the transistor at which current corresponding to the current of the second reference signal flows is M6, and the driving ability of the transistor at which current corresponding to the current of the input signal flows is M7,

a relationship M3 > M2 = M7 > M6 is established among the driving forces M2, M3, M6, and M7.

14. A semiconductor apparatus according to claim 10, wherein

the signal level of the second reference signal is

greater than the signal level of the first reference signal, and

among the pair of transistors for input of the first current comparison circuit, the driving ability of the transistor at which current corresponding to the current of the input signal flows is M2, and the driving ability of the transistor at which current corresponding to the current of the first reference signal flows is M3, and

among the pair of transistors for input of the second current comparison circuit, the driving ability of the transistor at which current corresponding to the current of the second reference signal flows is M6, and the driving ability of the transistor at which current corresponding to the current of the input signal flows is M7,

a relationship M6 > M2 = M7 > M5 is established among the driving forces M2, M3, M6, and M7.

15. A semiconductor apparatus according to claim 3, wherein the memory cell is a memory cell which makes a resistance value varying in accordance with a state of arranging magnetization of two magnetic layers of a magnetic resistive element having the two magnetic layers sandwiching a non-magnetic layer therebetween correspond to "0" and "1" data, and which generates induction magnetic flux by making current flow at a writing wire disposed close to the magnetic

resistive element, and which writes information by changing a direction of magnetization of a recording layer of the magnetic resistive element.

16. A signal transmission system which transmits and receives binary logic signals between a plurality of semiconductor apparatuses, wherein

the plurality of semiconductor apparatuses respectively have an input receiver that decides a logic level of an input signal from an exterior, and a first reference signal corresponding to a logic "1" level of the input signal and a second reference signal corresponding to a logic "0" level are supplied as reference signals for logic level decision to the respective input receivers.

17. A signal transmission system according to claim 16, wherein the plurality of semiconductor apparatuses are packaged on a same wiring board, and structure a semiconductor module.

18. A signal transmission system according to claim 16, wherein

each of the input receivers including:

a first comparison circuit which compares an input signal with a first reference signal corresponding to the logic "1" level, and which outputs a first differential signal;

a second comparison circuit which compares the input signal with a second reference signal

corresponding to the logic "0" level, and which outputs a second differential signal; and

a third comparison circuit which compares an output of the first comparison circuit and an output of the second comparison circuit, and which decides a logic level of the input signal.

19. A signal transmission system according to claim 16, wherein a signal level of the first reference signal is greater than a signal level of the second reference signal, and the signal level of the first reference signal is a value greater than a maximum value of a distribution of a signal level of the logic "1" level of the input signal, and the signal level of the second reference signal is a value less than a minimum value of a distribution of a signal level of the logic "0" level of the input signal.

20. A signal transmission system according to claim 16, wherein a signal level of the second reference signal is greater than a signal level of the first reference signal, and the signal level of the first reference signal is a value less than a minimum value of a distribution of a signal level of the logic "1" level of the input signal, and the signal level of the second reference signal is a value greater than a maximum value of a distribution of an input level of the logic "0" level.

21. A semiconductor apparatus comprising a logic

level decision circuit to which a first reference signal having a logic "1" level and a second reference signal having a logic "0" level are input as reference signals for deciding a logic level of an input signal having a binary logic, and which decides the logic level of the input signal in accordance with which of the signal levels of the first and second reference signals the signal level of the input signal is close to.